IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Bor-Wen CHAN, et al.	§	Attorney Docket No.: 2002-1399 / 24061.58
	§	
	§	Group Art Unit: 2811
Serial No.: 10/728,995	§	
	§	Examiner: Crane, Sara W.
Filed: December 5, 2003	§	
	§	Confirmation No.: 9115
For: MICROELECTRONIC DEVICE HAVING DISPOSABLE SPACER	§	
	§	

Mail Stop: Amendment
Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-FINAL OFFICE ACTION MAILED APRIL 7, 2006

I. Introductory Comments

This paper is submitted in response to the Non-Final Office Action mailed April 7, 2006. No fees, including extension of time fees, are believed necessary for consideration of the present paper. However, if any fees are necessary, including extension of time fees, the extension of time is hereby requested, and the Commissioner is hereby authorized to charge any fees, including those for the extension of time, to Haynes and Boone, LLP's Deposit Account No. 08-1394.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

II. Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method of manufacturing a microelectronic device, comprising:

forming a patterned feature over a substrate;

depositing a conformal polymer layer over the patterned feature and the substrate, wherein such depositing employs a fluorine-containing plasma source;

etching the polymer layer to expose the patterned feature and a portion of the substrate, thereby forming polymer spacers on opposing sides of the patterned feature; and

forming an insulating layer over the polymer spacers.

2. (Original) The method of claim 1 wherein the conformal polymer layer is deposited in a chemical reactive plasma environment.

3. (Original) The method of claim 1 wherein the substrate comprises diamond.

4. (Original) The method of claim 1 wherein the substrate comprises strained silicon.

5. (Original) The method of claim 1 wherein the patterned feature is a semiconductor device gate structure.

6. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises CF_4.

7. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises CF_3.

8. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises C_2F_2.

9. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises CH_2F_2.

10. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises CHF_3.

11. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises C_2F_6.

12. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises C_3F_8.

13. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises SF_6.

14. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises C_3F.

15. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises CH_3F.

16. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source comprises a fluorocarbon.

17. (Currently Amended) The method of claim 1 wherein a flow rate of the fluorine-containing ~~chemistry~~ plasma source ranges between about 5 sccm and about 200 sccm.

18. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source further includes a chlorine-containing gas.

19. (Original) The method of claim 18 wherein the chlorine-containing gas comprises Cl_2 and chlorocarbons.

20. (Currently Amended) The method of claim 1 wherein the fluorine-containing ~~chemistry~~ plasma source further includes a bromine-containing gas.

21. (Original) The method of claim 20 wherein the bromine-containing gas comprises HBr.

22. (Original) The method of claim 1 wherein the etching employs an oxygen-containing gas.

23. (Original) The method of claim 22 wherein the oxygen-containing gas comprises O_2.

24. (Original) The method of claim 22 wherein the oxygen-containing gas comprises O_3.

25. (Original) The method of claim 22 wherein the oxygen-containing gas comprises NO_2.

26. (Original) The method of claim 22 wherein the oxygen-containing gas comprises CO_2.

27. (Original) The method of claim 22 wherein the oxygen-containing gas comprises CO.

28. (Previously Presented) The method of claim 1 wherein the step of depositing the polymer layer employs a direct current (DC) bias applied to the substrate ranging between about 1 Watts and about 50 Watts.

29. (Previously Presented) The method of claim 1 wherein the step of depositing the polymer layer employs a radio frequency (RF) bias applied to the substrate ranging between about 1 Watts and about 50 Watts.

30. (Original) The method of claim 1 wherein the etching the spacer employs a direct current (DC) bias applied to the substrate ranging between about 1 Watts and about 500 Watts.

31. (Original) The method of claim 1 wherein the etching the spacer employs a radio frequency (RF) bias applied to the substrate ranging between about 1 Watts and about 500 Watts.

32. (Previously Presented) The method of claim 1 further comprising:
forming source/drain regions in the substrate on opposing sides of the patterned feature.

33. (Original) The method of claim 32 wherein removing the spacers includes etching the spacers with an oxygen-containing gas.

Claims 34-36 (Cancelled).

37. (Previously Presented) A method of manufacturing a microelectronic device, comprising:

forming a doped well in a substrate;

forming a gate stack over the doped well;

forming, in-situ, polymer spacers on opposing sides of the gate stack by:

employing a substrate bias and a fluorine-containing plasma source to deposit a conformal polymer layer over the gate stack; and

adjusting the substrate bias, without removing the substrate bias, to etch the polymer layer with the fluorine-containing plasma, thereby exposing the gate stack and defining the polymer spacers; and

forming an insulating layer over the polymer spacers.

38. (Previously Presented) The method of claim 37 wherein forming the doped well includes:

employing a high density plasma source to form the doped well, the high density plasma source having a carbon-to-deuterium ratio ranging between about 0.1 percent and about 5 percent in a process ambient, wherein the process ambient pressure ranges between about 0.1 mTorr and about 500 Torr and the substrate is held at a temperature ranging between about 150°C and about 1100°C; and

treating the doped well by employing a deuterium-containing plasma.

39. (Previously Presented) The method of claim 37 further comprising:

forming source/drain regions in the doped well via ion implantation before the step of forming the insulating layer, wherein forming the source/drain regions includes employing the polymer spacers to laterally limit formation of the source/drain regions during the ion implantation; and

forming contact regions over the source/drain regions and contacting the polymer spacers, before the step of forming the insulating layer.

III. Remarks

Reconsideration of this application in light of the above amendments and the following remarks is requested.

Claims 1-36 were originally filed in the present application. Claims 34-36 were subsequently cancelled without prejudice or disclaimer in response to a restriction requirement.

Claims 7-15 and 24-27 were previously withdrawn from consideration in response to an election requirement. However, these claims are now under consideration because the Examiner has withdrawn the election requirement.

The amendment which accompanied the subsequent Request for Continued Examination added claims 37-39.

No claims are currently added or canceled in the present paper. Consequently, claims 1-33 and 37-39 remain pending and under consideration.

Applicants also note with appreciation the Examiner's indication that claims 37-39 have been allowed.

IV. Rejections under 35 U.S.C. § 112

Claims 1-33 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Specifically, the claims are ambiguous as the result of a typographical error repeated in each of claims 6-18 and 20. That is, each of these claims recited "fluorine-containing chemistry" for which there was no antecedent basis in the base claim, independent claim 1. However, claims 6-18 and 20 are currently amended to correct this inadvertent error, by amending "fluorine-containing chemistry" to "fluorine-containing plasma source," for which antecedent basis properly exists. Applicants note with appreciation the Examiner's assistance in correcting this error.

V. Conclusion

It is believed that all matters set forth in the Office Action have been addressed. Favorable consideration and an early indication of the allowability of the claims are respectfully requested. Should the Examiner deem that an interview with Applicants' undersigned attorney would expedite consideration, the Examiner is respectfully invited to call the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

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Dated: 6/19/06

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I hereby certify that this correspondence is being filed with the U.S. Patent and Trademark Office via EFS-Web on June 19, 2006.

Bonnie Boyle